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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/663,917

09/17/2003

Takeshi Akatsu

4717-8900

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28765

7590

11/17/2004

WINSTON & STRAWN
PATENT DEPARTMENT
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EXAMINER

PERKINS, PAMELA E

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/663,917

Applicant(s)

AKATSU ET AL.

Examiner

Pamela E Perkins

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) 21-25 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/17/03, 4/27/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 17 September 2003. Claims 1-25 are pending.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-20, drawn to a method of manufacturing a semiconductor wafer, classified in class 438, subclass 481.
- II. Claims 21-25, drawn to a semiconductor wafer, classified in class 257, subclass 19.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process. For example, the product as claimed does not require obtaining a production wafer and donor wafer by splitting a composite structure, as required by the process as claimed.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Allen Fanucci on 22 March 2004 a provisional election was made without traverse to prosecute the invention of group I, claims 1-20 drawn to a method of manufacturing a semiconductor wafer. Affirmation of this election must be made by applicant in replying to this Office action. Claims 21-25 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3 and 18 are rejected under 35 U.S.C. 112, second paragraph, as there is insufficient antecedent basis for this limitation in the claim.

Claims 3 and 18 recites the limitation "the first implantation location" in lines 2 & of claim 3 and line 2 of claim 18. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maa et al. (6,780,796) in view of Sakaguchi et al. (6,534,382).

Maa et al. disclose a method of preparing crystalline wafer where a first composite structure comprises a support substrate (10) and a first epitaxial layer (12) that is in a strained state and is associated with one side of the support substrate (10) (col. 3, lines 43-59); and relaxing the strained state of the first epitaxial layer (12) of the composite structure to an at least partially relaxed state by providing dislocations in a dislocation layer within the first composite structure in a configuration sufficient to relax the first epitaxial layer (12) to a substantially relaxed state (col. 3, line 60 thru col. 4, lines 19). Maa et al. further disclose forming a strained silicon (22) over the epitaxial layer and the support substrate (10) as a semiconductor wafer (col. 4, lines 24-26). Referring to claim 12, Maa et al. disclose the support substrate (10) comprising silicon (col. 3, lines 43-52).

Referring to claim 13, Maa et al. disclose the first epitaxial layer (12) comprising silicon germanium (col. 3, lines 52-59).

Referring to claim 16, Maa et al. disclose the dislocations are provided by implanting atomic species in the first composite structure in a dosage sufficient to facilitate or relax the first epitaxial layer (12) to the relaxed state (col. 3, lines 24-42).

Referring to claim 19, Maa et al. disclose where energy is added to the first composite structure to relax the first epitaxial layer (12) (col. 4, lines 9-19).

Referring to claim 20, Maa et al. disclose the dislocation layer is disposed in the support substrate (10) (col. 3, lines 24-42).

Maa et al. do not disclose associating a receiving substrate with the first composite structure with the side of the support that includes the first epitaxial layer; and obtaining a production wafer and a donor wafer by splitting the first composite structure at a region of weakness located therein.

Sakaguchi et al. disclose a method of preparing crystalline wafer where a first composite structure comprises a support substrate (701) and a first epitaxial layer (702) associated with one side of the support substrate (701) (Fig. 8A); associating a receiving substrate (705/706) with the first composite structure with the side of the support that includes the first epitaxial layer (702); and obtaining a production wafer (706) and a donor wafer (701) by splitting the first composite structure at a region of weakness located therein (Fig. 8D; col. 11, lines 44-52 & line 61 thru col. 12, line 5; col. 19, lines 27-67). Sakaguchi et al. further disclose creating the region of weakness by implanting atomic species at an implantation location (col. 25, lines 18-48).

Referring to claim 4, Sakaguchi et al. disclose the region of weakness is disposed in the support substrate (Fig. 8FB; col. 25, lines 42-48).

Referring to claim 5, Sakaguchi et al. disclose the region of weakness is disposed in the first epitaxial layer (Fig. 8FA; col. 25, lines 32-37).

Referring to claim 6, Sakaguchi et al. disclose providing an additional layer (704) on the first epitaxial layer (702) prior to associating the receiving substrate (705/706) with the first composite structure, wherein the receiving substrate (705/706) is bonded to the additional layer (703) (Fig. 8B & 8C; col. 27-50).

Referring to claim 9, Sakaguchi et al. disclose removing a layer (704) of the production wafer (706) disposed on an opposite side of the first epitaxial layer (702) from the receiving substrate (705/706) to provide an exposed surface (Fig. 8FA & 8FB; col. 19, lines 51-55).

Referring to claim 10, Sakaguchi et al. disclose providing another layer on the exposed surface of the production wafer (2000) (Fig. 4; col. 15, lines 6-63).

Referring to claim 11, Sakaguchi et al. disclose the another layer is grown on the exposed surface (col. 15, lines 6-63).

Since Maa et al. and Sakaguchi et al. are both from the same field of endeavor, a method of preparing crystalline wafer, the purpose disclosed by Sakaguchi et al. would have been recognized in the pertinent art of Maa et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Maa et al. by associating a receiving substrate with the first composite structure with the side of the support that includes the first epitaxial layer; and obtaining a production wafer and a donor wafer by splitting the first composite structure at a region of

weakness located therein as taught by Sakaguchi et al. Sakaguchi et al. to prevent contamination of the epitaxial layer (col. 7, lines 40-62).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maa et al. in view of Sakaguchi et al as applied to claim 1 above, and further in view of Yoshida (6,787,793).

Maa et al. in view of Sakaguchi et al. disclose the subject matter claimed above except relaxing the first epitaxial layer sufficiently to reduce the strain thereof to less than 75% of the strain than in the strained state.

Yoshida discloses a method of preparing crystalline wafer where a first composite structure comprises a support substrate (1) and a first epitaxial layer (2) that is in a strained state and is associated with one side of the support substrate (1); relaxing the strained state of the first epitaxial layer (2) of the composite structure to an at least partially relaxed state (col. 6, lines 56-66). Yoshida further discloses relaxing the first epitaxial layer (2) sufficiently to reduce the strain thereof to less than 75% of the strain than in the strained state (Fig. 3; col. 5, lines 18-29).

Since Maa et al. and Yoshida are both from the same field of endeavor, a method of preparing crystalline wafer, the purpose disclosed by Yoshida would have been recognized in the pertinent art of Maa et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Maa et al. by relaxing the first epitaxial layer sufficiently to reduce the strain thereof to less than 75% of the strain than in the strained state as taught by Yoshida to increase mobility and improve smoothness (col. 1, lines 25-48; col. 2, lines 58-67).

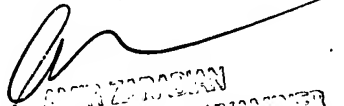
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP


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